



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

*[Handwritten Signature]*

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,426	03/26/2004	Hideki Shioe	559502001200	2605
25226	7590	08/23/2005		EXAMINER
MORRISON & FOERSTER LLP 755 PAGE MILL RD PALO ALTO, CA 94304-1018				NGUYEN, KHANH V
			ART UNIT	PAPER NUMBER
			2817	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/811,426	SHIOE, HIDEKI	
Examiner	Art Unit		
Khanh V. Nguyen	2817		

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)  Responsive to communication(s) filed on 26 March 2004.

2a)  This action is **FINAL**.                            2b)  This action is non-final.

3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

4)  Claim(s) 1-12 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5)  Claim(s) \_\_\_\_\_ is/are allowed.  
6)  Claim(s) 1-12 is/are rejected.  
7)  Claim(s) \_\_\_\_\_ is/are objected to.  
8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

9)  The specification is objected to by the Examiner.

10)  The drawing(s) filed on 26 March 2004 is/are: a)  accepted or b)  objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a)  All    b)  Some \* c)  None of:  
1.  Certified copies of the priority documents have been received.  
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_.  
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)  Notice of References Cited (PTO-892)  
2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3)  Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 3/26/04.

4)  Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.  
5)  Notice of Informal Patent Application (PTO-152)  
6)  Other: \_\_\_\_\_

## DETAILED ACTION

### *Drawings*

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "PNP transistor" and "NPN transistor" in claims 7, 8 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 4, 5, 7, 8, 10-12 recite the limitation "the outside" in line 6. There is insufficient antecedent basis for this limitation in the claim.

Regarding claims 1, 12, it is not clear which "the outside" is intended.

Regarding claims 3, 5, lines 5 and 6 respectively, it is not clear which "the base current" is intended since there are "base current control section" and "base current supply section" disclose in the claims.

Claims 7, 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 7, it is not clear which "output transistor is a PNP transistor" is intended having its emitter which is grounded as claimed in claim 1.

Regarding claim 8, it is not clear which "comparator is an NPN transistor" is intended. Note, Figures disclose comparator (Q7, Q8) which is PNP type and not NPN as claimed. And comparator is made up of at least two transistors not a single transistor as claimed.

Regarding claims 10, 11, which also depended on claim 3, wherein neither claims 1 and 3 having any type of amplifier claimed.

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mavencamp (6,175,277).

Regarding claims 1, 2, Mavencamp discloses the claimed invention except utilizing bipolar type transistor (base, emitter and collector) as claimed. Mavencamp utilizes field effect transistor (FET) having gate, drain and source. Mavencamp (Figs. 1, 2) discloses an output stage comprising: an output transistor (314) having source (emitter) grounded, a gate (base) serves as an input node for control current and a drain (collector) serves as output node (OUTPUT B); an input stage (20) of Fig. 1 can be read as a gate (base) current supply section; and transistor pair (350, 352) can be read as a gate (base) current control section for detecting an inter-terminal voltage (OUTPUT B) and comparing inter-terminal voltage (OUTPUT B) with a predetermined voltage (INPUT A), wherein transistor pair (350, 352) operable as a comparator. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted the field effect transistors of Mavencamp with bipolar transistors, since such a modification is well known and considered a mere substitution of art-recognized equivalent transistors.

Regarding claims 3-5, 10, 11, wherein the gate (base) current control section supplies a first control current via transistors (332, 330, 334, 336) and a second control current via transistors (370, 372) and control gate (base) of output transistor (314) via a node, wherein transistors form plurality of current mirrors.

Regarding claim 6, wherein the output transistor (314) is a N-type.

Regarding claim 9, wherein the comparator (350, 352) is PNP type.

Regarding claim 12, Mavencamp discloses the claimed invention except utilizing bipolar type transistor (base, emitter and collector) as claimed. Mavencamp utilizes field effect transistor (FET) having gate, drain and source. Mavencamp (Figs. 1, 2) discloses an output stage comprising: an NPN output transistor (314) an source (emitter) of which is connected to a first power supply potential (ground), a gate (base) of which serves as an input node for a control current, and a drain (collector) of which serves as an output node (OUTPUT B); a PNP output transistor (310) an source (emitter) of which is connected to a second power supply potential, a gate (base) of which serves as an input node for a control current and a drain (collector) of which serves as an output node (OUTPUT B) in common to the PNP output transistor (310) and the NPN output transistor (314); a first base current supply section (332, 330, 334, 336, 370, 372) for supplying a base current to the NPN output transistor (314) according to an input signal (INPUT A); a first base current control section (350, 352) for detecting a first inter-terminal voltage between the collector and emitter of the NPN output transistor to control a base current supplied from the first base current supply section so as not to cause the first inter-terminal voltage to fall to a value lower than a first predetermined voltage; a second base current supply section (322, 320, 324, 326, 362) for supplying a base current to the PNP output transistor (310) according to the input signal; and a second base current control section (340, 342) for detecting a second inter-terminal voltage between the collector and emitter of the PNP output transistor to control a base current supplied from the second base current supply section so as not to cause the

second inter-terminal voltage to fall to a value lower than a second predetermined voltage. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted the field effect transistors of Mavencamp with bipolar transistors, since such a modification is well known and considered a mere substitution of art-recognized equivalent transistors.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh V. Nguyen whose telephone number is (571) 272-1767. The examiner can normally be reached from 8:00 AM - 3:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



**KHANH V. NGUYEN  
PRIMARY EXAMINER**